

**TITLE: A METHOD AND APPARATUS FOR PROVIDING AN INTER
INTEGRATED CIRCUIT INTERFACE WITH AN EXPANDED
ADDRESS RANGE AND EFFICIENT PRIORITY-BASED DATA
THROUGHPUT**

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FIELD OF THE INVENTION

The present invention relates to Inter Integrated Circuit (I2C) interface addressing for communication between connected devices. In particular, the invention provides
10 implementation of a larger address space. Additionally, the invention permits efficient high priority accesses.

BACKGROUND OF THE INVENTION

As is well known in the prior art, an I2C (Inter-IC) bus is a bi-directional two-
15 wire serial bus that provides a communication link between devices connected to the bus. Devices are typically considered as masters or slaves when data transfers are being performed. The master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

20 Fig. 1 illustrates the prior art, 7-bit protocol used in I2C bus communications. This protocol is fairly simple, with a five-part format comprising: 1) A start bit 102 to initiate a transaction, 2) an address byte, with seven bits 104 denoting the address of the slave device and the eighth bit 106 denoting a read or write command, 3) data bytes 108, 4) an acknowledge bit 110 following each 8-bit address or data byte, and 5) a stop bit 112
25 to terminate the transaction.

Not illustrated in Fig. 1 is another, prior art protocol that uses a 10-bit addressing protocol in which the slave address 104 has the format 11110XX (as before, the eighth bit of this information byte is a read/write indicator 106). The five high order bits indicate that 10-bit addressing protocol is being employed, while the remaining two bits are the

two high order bits of the slave address. The remaining 8 bits of the 10-bit address are then provided in the first data byte 108.

Both these 7-bit and 10-bit prior art addressing protocols permit an additional data byte 108 to contain additional addressing information, such as an internal register address
5 of the slave device.

Although widely used, the I2C bus suffers from several drawbacks, one of which is the limited addressability / time inefficiencies inherent in its protocol. Prior art attempts at remedying this problem have chiefly involved adding external pins to the slave device. While this method does permit the I2C master to control a larger word
10 addressing space, it requires larger package pin counts for any I2C slave devices to be so addressed.

The current invention provides access to a large address space without requiring additional external pins on the device addressed. Further, the invention provides an interface that is efficient for high priority accesses.
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SUMMARY OF THE INVENTION

This invention relates to an enhanced protocol between an I2C master device and an I2C slave device. In various embodiments, the invention permits greater addressable space and high priority access to the slave device. The enhanced protocol is implemented
20 by the addition of command code data being transmitted immediately following the 7-bit slave address (+ 1 bit read/write indicator) used in the conventional 7-bit addressing protocol.

The addressed slave device would recognize the command code through an interface circuit inside the slave device. A large system, of which the master and slave
25 are components, would be configured such that devices seeking to address that slave device would know to do so in the enhanced protocol format. Configuring of system components as to required communication protocols in this manner is well-known in the prior art.

Various embodiments of the invention permit alternative addressing schemes to be implemented by this command code structure. In particular, the invention provides an I2C solution for accessing high priority address space with one command byte, medium priority space with two command bytes and low priority space with three command bytes.

BRIEF DESCRIPTION OF THE DRAWINGS

Various embodiments of the present invention will now be described in detail in conjunction with the annexed drawings, in which:

FIG. 1 illustrates the basic protocol in an I2C bus write operation in accordance with the prior art;

FIG. 2 illustrates a block diagram of an I2C bus structure connecting master and slave devices;

FIG. 3 illustrates an I2C interface circuit according to an embodiment of the invention;

FIG. 4 illustrates an exemplary write operation enhanced protocol for 14-bit addressing (low priority) according to an embodiment of the invention;

FIG. 5 illustrates an exemplary write operation enhanced protocol for 6-bit addressing (medium priority) according to an embodiment of the invention; and,

FIG. 6 illustrates an exemplary write operation enhanced protocol for direct command (high priority) according to an embodiment of the invention.

DETAILED DESCRIPTION

The present invention describes an enhanced priority access data protocol between an I2C master device and an I2C slave device. Fig. 2 illustrates an embodiment of the invention in which an I2C bus structure connects a master device 202 and a slave device 204. The two devices communicate through the data line, SDATA 206 and clock line, SCLK 208. As illustrated, and as is typical in the prior art, the master 202 provides the clock during the communication session while both devices, through the I2C standard protocol, drive data.

In this embodiment of the invention, an enhanced I2C protocol is implemented through an interface circuit 210 contained in the slave device. This interface circuit 210 not only communicates with the bus but with various internal memories 212, internal registers 214, and internal devices (e.g., PLL 216) of the slave device 204.

5 Fig. 3 illustrates the interface circuit 210 in greater detail. As depicted, the interface circuit 210 consists of the following blocks: an I2C_detect block 302 to detect start and stop condition; an I2C_datapath block 304 to transfer data back and forth to internal registers, memories, and devices; an I2C_protocol block 306 to generate the transitions from one priority state to another and an I2C_control block 308 to generate the
10 I2C control signals to the I2C_datapath block 304. As further depicted in Fig. 3, I2C_datapath block 304 communicates with the slave device through various signaling channels. Items 312 and 314 denote 8-bit data_in and 8-bit data_out channels, respectively. Items 320 and 322 denote read enable and write enable 1-bit signaling, respectively. The use of such signaling is well known in the prior art. In the illustrated
15 embodiment, internal_address 310 is a 14 bit address. As shall be described below in greater detail, in the event the address protocol of the present invention does not utilize all 14 bits, the high order bits are simply padded with zeroes. Fig. 3 also depicts a wr_softreset signal line 318 and a wr-command bit signal 316 which are used in the protocol of the current invention to perform a direct command function. This function
20 will be described in greater detail below in the discussion of Fig. 6.

In an embodiment of the invention to be discussed now in greater detail, the enhanced protocol is implemented by augmenting the prior art I2C 7-bit addressing protocol illustrated in Fig. 1. This augmentation is implemented by the creation and transmission of a sequence or array of addressing parameters. In particular, an 8-bit
25 command code is transmitted immediately following the slave address 104 and the R/W indicator 106. The low order 6 bits of this command code contain a supplemental address which will be used in addressing an internal location within the slave device. The first two bits of this command code are used to denote which of three addressing schemes of this embodiment of the invention are being implemented: (1) 14-bit addressing, (2) 6-bit

addressing and (3) direct command access. These addressing schemes correspond to Figs. 4, 5 and 6, respectively. Each will now be discussed in greater detail.

Fig. 4 illustrates an exemplary write operation using the enhanced protocol of this embodiment of the invention wherein low priority, 14 bit addressing is implemented. As shown in Fig. 4, after a START condition 102, a 7-bit slave address 104 is transmitted first, followed by an R/W indicator bit 106. As illustrated, the R/W indicator 106 is depicted as a "0", thereby signaling that a write operation is to occur. If the 7-bit address matches the slave address, the I2C_protocol_block 306 acknowledges the master device 202 with an ACK bit 110 set to "0". The signaling depicted in Fig. 4 that has been discussed to this point, matches the conventional I2C protocol depicted in Fig. 1.

As illustrated in Fig. 4, the master device 202 next transmits an 8-bit command code 402. The interface circuit 210 monitors the upper two bits [7:6] of this command code 402. As depicted in Fig. 4, the status of these two bits is "01", thereby indicating a 14-bit address format is being communicated. In this case, the supplemental address consists of the lower 6 bits [5:0] of the 8-bit command code 402 and represents the upper 6 bits [13:8] of the 14-bit address being transmitted. Referring to Fig. 2, this 14-bit address is used by the Interface Circuit 210 to access an internal address of the slave device, i.e., a memory address 212, and internal register 214 or a Phase Lock Loop (PLL) device 216.

Next, and as is conventional in I2C protocol, upon receipt of an 8-bit byte of information, an acknowledgment (ACK 110) is sent by the slave device 204. The interface circuit 210 then receives the additional byte of address information -- the lower 8 bits [7:0] of the 14-bit internal address. As before, an ACK 110 signal is sent to acknowledge receipt of this byte of information. Communication then occurs in accordance with conventional I2C protocol. That is, the master device 202 starts writing data bytes 108 one byte at a time with the slave device 204 sending an ACK 110 indicator as they are received. As is well-known in the prior art, the word internal address registers or word internal memories are automatically incremented by one after each data byte transfer. Thus, by way of example, a write operation in which a plurality

of data bytes is to be written to a slave device's internal memory requires only the address of a starting memory location need be supplied. Also as is well-known in the prior art, the slave device 204 will remain addressed until it receives a STOP condition 112.

5 Fig. 5 illustrates an exemplary write operation according to this embodiment of the invention when the upper two bits [7:6] of the 8-bit command code 402 have a "00" status. This indicates that a 6-bit address format is being communicated, wherein the supplemental address, consisting of the lower 6 bits [5:0] of the command code 402, is the 6-bit internal address. As in Fig. 4, the slave interface circuit 210 will generate an
10 ACK 110 in the 9th bit position indicating to the master device 102 that the byte of information 402 has been received. The I2C_protocol block 306 within the interface circuit 210 will have recognized that the next byte of information to be received will be data (as opposed to additional address information as in the example depicted in Fig. 4). Accordingly, it will cause the I2C_control block 308 and the I2C_datapath block 304 to
15 timely transition to the appropriate state to receive this data byte (and any subsequent data bytes) transmitted from the master device. As before, the word internal address registers are automatically incremented by one after each data byte 108 transfer. Also as before, the slave will remain addressed until it receives a STOP condition 112.

Both the 14-bit address illustrated in Fig. 4 and the 6-bit address illustrated in Fig.
20 5 represent an internal address of registers or internal memories of the slave device 204 being addressed. In a further embodiment of the invention (not illustrated), the interface circuit 210 would process these separate protocol formats in a similar manner as if both contained a 14-bit address. That is, upon recognizing a "00" command (indicating a 6-bit address is being transmitted), the interface circuit 210 would set each of the upper bits
25 [13,6] of the internal address to "0" and then employ the same internal 14-bit addressing algorithm in the slave device 204. Thus, as illustrated in Fig. 3, internal_address 310 would be represented as a 14-bit address regardless of which addressing scheme was used in the protocol.

The enhanced protocol also can be used to support a high priority write operation to selected registers contained in the slave device, as illustrated in Fig. 6. Specifically, when the upper two bits [7:6] of the 8 bit command are set to “11”, this may indicate to the interface circuit that the communication is a direct command access. In such a case, the lower 6 bits [5:0] of the 8-bit command code 402 are encoded to perform a write of predefined data to one of the selected registers. That is, this portion of the command code contains an address associated with a register in the slave device, which address, when accessed, will cause the loading of predetermined data into that register via a hard-coded internal write operation.

This high priority write operation would speed up writing data to selected registers or devices inside the slave device. An example of a useful application of this feature would be the resetting of a specific device contained in the slave device. In particular, the feature would enable selection of different frequency ranges of a PLL inside the slave device or switching of an internal multiplexing clock. Implementation of these examples is attained in an embodiment of the invention in which the command code 402 contains the low order 6 bits as indicated in Table 1:

Table 1 Direct Command Bits[5:0] Encoding

Bits[5:0]	Description
000000	Select frequency range 0
000001	Select frequency range 1
000010	Select frequency range 2
000011	Select frequency range 3
000100	Select frequency range 4
000101	Select frequency range 5
000110	Switch to Crystal clock
000111	Switch to PLL clock
001000	Softreset command
001001-111111	Reserved

It will be understood that the forgoing description of the invention is by way of example only, and variations will be evident to those skilled in the art without departing from the scope of the invention, which is as set out in the appended claims.